Abstract of the Disclosure

In an array-type processor in which a multiplicity of processor elements, which each execute data processing in accordance with instruction codes in which data are individually set, are arranged in rows and columns, and in which state control units cause successive transitions of the operating states of this multiplicity of processor elements for each operating cycle by means of contexts that are make up by instruction codes, a plurality of element areas are respectively connected to an equal number of state control units, and state control units that correspond to a prescribed number of operating states that are set to one context temporarily halt the operation of element areas to which the state control unit is connected during operating cycle in which operating states do not occur.